Testability & repair

EDM Event 16/09/2010
Imec
Leuven

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Testability & repair : agenda

- Testability / test coverage ?
  - How good is the board tested ?
    - 0% → 100 %
      - About the product
        EDM approach
  - Performance of the test ?
      - About the test
        example in test development
- PB free Repair
  - Consequences for choice of laminates ?
    - Examples

Testability & repair

- What tests are it about ?

  1. Production tests

  – Production tests to decide if a PBA is “OK” = is functioning
    - Intermediate and final PASS/FAIL
      – Tests to take out faulty PBA ‘s out of the production cycle, preventing to produce and deliver bad products.

  – Diagnostic tests to find the cause to solve the problem,
    - more extensive testing.
      – Tests to help repairing the board

  2. After sales repair (RMA)

  - Tests evaluate the PBA (GO/NOGO)
  - Diagnostic tests to find the cause

Testability

How do we know we have a good PBA ?

Production :

Different tests looking for different kinds of failures (defect type)

Production faults :

non-powered tests :
e.g. Vision tests :
looking for “ missing : misoriented components , solderbridges , opens , …

MDA tests

powered tests :
structural tests

functional tests.

Testability Test coverage (EDM)

- **Testcoverage per defecttype DOi (IPC-7912) .**

IPC Defect category (Termination, Placement , component , Assembly) en IPC Defect Types.

Each DOi has

- **TestAccess Value : TA**
- **Test efficiency : TE**

- **A Test Coverage Value : TC = TA * TE**

absolute testcoverage per defect opportunity
Ponderated Test Coverage
Equivalent Test Coverage
Test Coverage per defect Category .
Test Coverage of the PBA
Absolute test coverage

$$ATC_i = \frac{\sum_{k=i}^{N\,i} TC_i^k}{N_i}$$

Testability Testcoverage (very) simple approach

tested net : e.g. measure 5V on testpoint → 5V source OK

net testability = 100 % ?

net coverage = ?

Test access / coverage

widely used in functional testing

Testability & Test coverage on test development systems
Electrical test

Testability = theorectical maximum coverage

Net testability / coverage   Pin testability / coverage

- The **pin** testability is calculated as follows:

0% : Pins that cannot be tested at all

50% : Pins that can sense only 1 or 0 (Pwr, Gnd)
Pins that can drive only 1 or 0

100% : Pins that can sense 1 and 0
Pins that can drive 1 and 0

- **The net testability is the weighted sum of pintestability of pins in a net : ΣPin%/n.**
- **The percentage for the actual fault coverage is what is covered by the tests.**

Testability & Test coverage test development systems
Electrical test

Net Name	Pin Testability	%	Net Testability	Pin Coverage	Net Coverage
PCE1#			100%		33%
Z5, 1	Sense and Drive (external)	100%		0%	
IC14, M6 (IO_81)	Sense and Drive	100%		50%	
IC1, 19 (2B4)	Sense and Drive (indirect)	100%		50%	
PB_RST#			67%		0%
OSC_EN			0%		0%

ΣPin%/n.

ΣPin%/n.

- ➢ Single net :
  - – Improve test coverage : test development
  - – Improve testability HW design –
    - PBA + testaccess
      testinterface

Testability & Test coverage test development systems
Electrical test

- Testability and Actual test coverage define the possibility to detect a failure .

  GO / NOGO or PASS/FAIL tests

  - Testability   = Pba design issue
  - Testcoverage = test development (design) issue

- Necessary but not sufficient condition to locate a failure

  - In **this** example one single net with different connections (terminals/pins) is checked.
    - Opens , stuck at faults are 100 % detected and located
    - Bridges are found depending on the test(s)
      (subsets of nets are important)

Repair :

- Repair is a corrective action based on
  - effective fault detection/location
    - For Expected faultspectrum
    - Diagnostic tooling (testsystems)
  - Experience (repair database)
  - Trial & error
- In many cases a solderprocess occurs

Repair : expected fault spectrum

	production	repair
design failures	✓	✓
Manufacturing failures		
Analog nets		
opens	✓✓	✓✓
bridges	✓✓	✓
stuck at 0/1	✓✓	✓
Wrong analog components	✓✓	
Missing analog components	✓✓	
Bad orientation of components	✓✓	
(Complex) Digital nets	✓✓	
opens	✓✓	✓
bridges	✓✓	
stuck at 0/1	✓✓	✓
Wrong digital components	✓✓	
Missing digital components	✓✓	✓
Bad orientation of components	✓✓	
wrong programmed device	✓✓	✓
Defective Components		
analog	✓	✓✓
digital	✓	✓✓

Repair : effective fault detection/location

	F-test	BST	Vision	MDA/FP	ICT
design failures	☺	☺	☹	☹	☹

Manufacturing failures					
Analog nets	😐	😐	☹	☺	☺
opens	😐	😐	☹	☺	☺
bridges	😐	😐	☹	☺	☺
stuck at 0/1	😐	😐	☹	☺	☺
Wrong analog components	😐	😐	😐	☺	☺
Missing analog components	😐	😐	☺	☺	☺
Bad orientation of components	😐	😐	☺	☺	☺
(Complex) Digital nets	😐	☺	☹	😐	😐
opens	😐	☺	☹	😐	😐
bridges	😐	☺	☹	😐	😐
stuck at 0/1	😐	☺	☹	😐	😐
Wrong digital components	😐	☺	☹	😐	😐
Missing digital components	😐	☺	☹	😐	😐
Bad orientation of components	😐	☺	☹	☺	😐
wrong programmed device	😐	☺	☹	😐	😐

Defective Components					
analog	😐	😐	☹	☹	☺
digital	😐	😐	☹	☹	☺

depends on probe access	
can be detected	😐
strong feature	☺
probably not detected	☹

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Available testsystems

	F-test	BST	Vision	MDA/FP	ICT
production	☺	☺	☺	☺	☺
RMA repair	☺	☺	☹	☹😐	☹

Repair : solder process

- One must garantee that the PBA can survive one or more additional solder process cycles.

- Is this important for the choice of laminate ?

Production cycle without any repair activity.

- Application of EDM design guide for
  - a digital board NiAu finish with different BGA 's
  - Digital / analog PBfree HAL finish

  Assumption :

  - standard reflow soldercycle (max. Temp 260°C)
  - IPC category / classes

Category	Td (°C)	T260 (min)	T288 (min)	T300 (min)	CTEz (%)	Potentially Compliant Classes
Basic	310	30	5	AABUS	4	/99,/101,/102,/103,/121,/122, /124,/125,/126,/127,/128,/129, /130,/131
Mid	325	50	10	AABUS	3.5	/99,/102,/103,/124,/125,/126, /128,/129,/130,/131
High	340	80	15	2	3	/102,/126,/130 /129 (except *CTEz*=3.5%), /131 (except *CTEz*=3.5%)

No repair action required

PCB	Digi1	mm
Thickness	D	1,6
Drilled hole diameter	d	0,2
plating thickness	t	0,02
Via Stress Factor	**VSF**	**9,86**

Process		Counts for
NiAu		0
Reflow		2
Manual soldering		1
1 Component replacement (BGA)		0
Safety margin		NA
Number of temp. cycles	**Sn**	**3**

Category	Basic

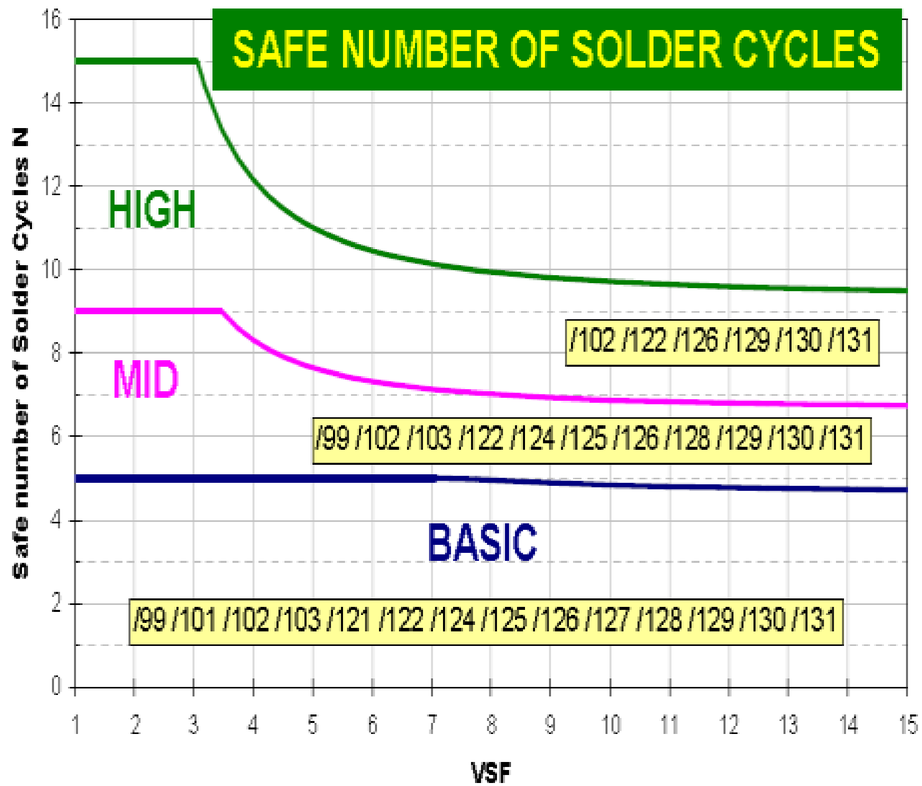

Figure I.16: Safe number of solder cycles for the three thermal performance classes.

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Repair: 1 component replacement

PCB	Digi1	mm
Thickness	D	1,6
Drilled hole diameter	d	0,2
plating thickness	t	0,02
Via Stress Factor	**VSF**	**9,86**

Process		Counts for
NiAu		0
Reflow		2
Manual soldering		1
1 Component replacement (BGA)		3
Safety margin		NA
Number of temp. cycles	**Sn**	**6**

Category	**MID**

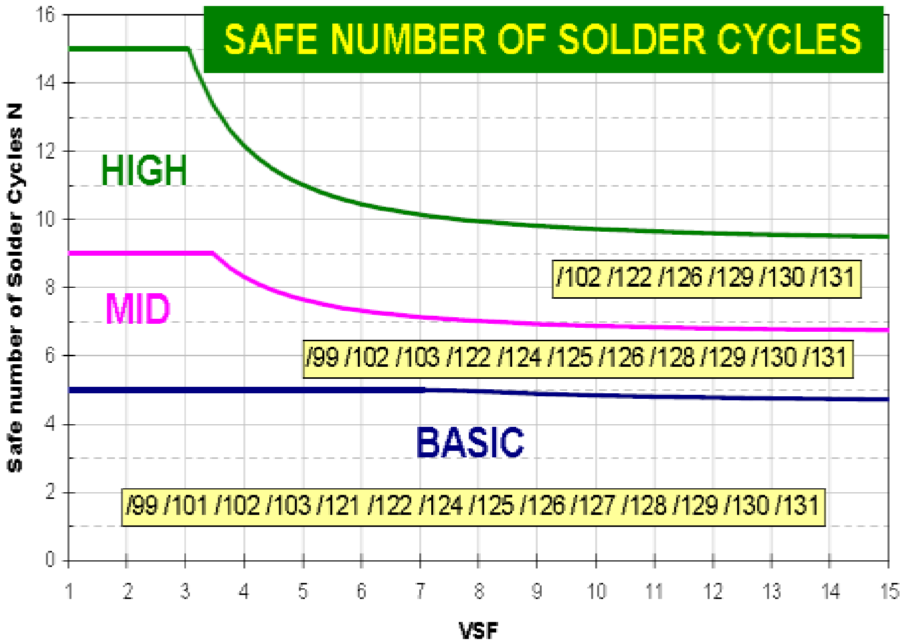

Figure I.16: Safe number of solder cycles for the three thermal performance classes.

1 Component replacement + RMA repair

PCB	Digi1	mm
Thickness	D	1,6
Drilled hole diameter	d	0,2
plating thickness	t	0,02
Via Stress Factor	**VSF**	**9,86**

Process		Counts for
NiAu		0
Reflow		2
Manual soldering		1
1 Component replacement (BGA)		3
Safety margin		NA
Number of temp. cycles	**Sn**	**6**

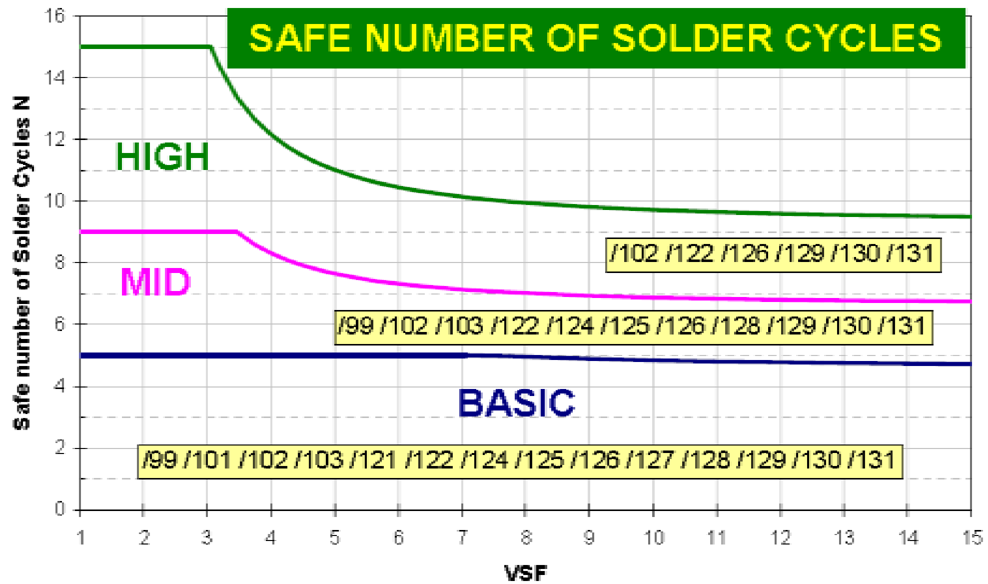

Figure I.16: Safe number of solder cycles for the three thermal performance classes

RMA process

Process		Counts for	
1 Component replacement (BGA)		3	
2 Component replacement (BGA)			6
Number of temp. cycles	Sn	**9**	**12**

Category		**HIGH**	**???**

Example : powerboard

PCB	power1	mm
Thickness	D	1,6
Drilled hole diameter	d	0,37
plating thickness	t	0,02
Via Stress Factor	VSF	**8,94**

Process	Counts for
HASL finish	2
Reflow	1
Wave solder	1
Touch up repair	1
Sn	**5**
Result:	**BASIC-MID**

repair action	
Component replacement	3
Sn	**8**
Result:	**High**

Field return	
Component replacement	3
Sn	**11**

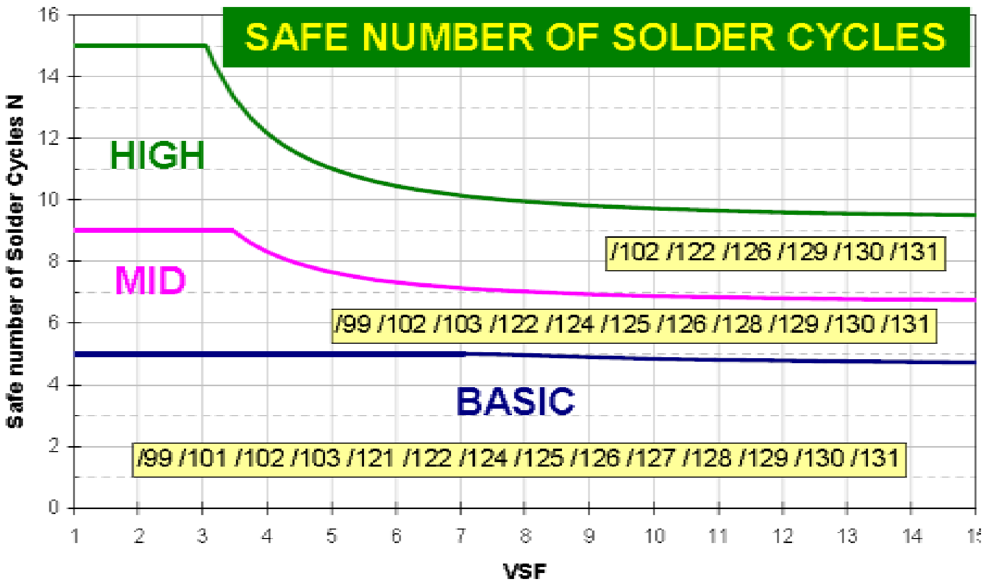

Figure I.16: Safe number of solder cycles for the three thermal performance classe

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Via Stress Factor	VSF	**8,94**

Process	Counts for
HASL finish	2
Reflow	1
Wave solder	1
Touch up repair	1
Sn	**5**
Result:	**BASIC-MID**

repair action	
Component replacement	3
Sn	**8**
Result:	**High**

Field return	
Component replacement	3
Sn	**11**
Result:	**??**

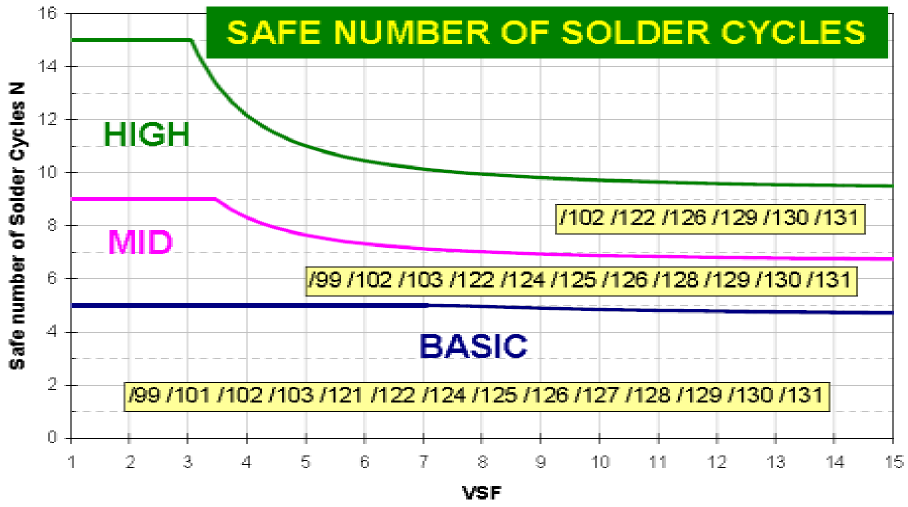

Figure I.16: Safe number of solder cycles for the three thermal performance classes.

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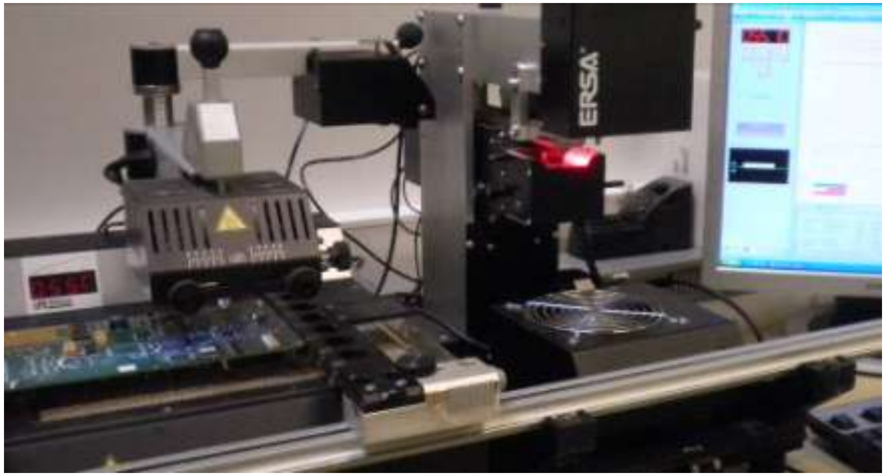
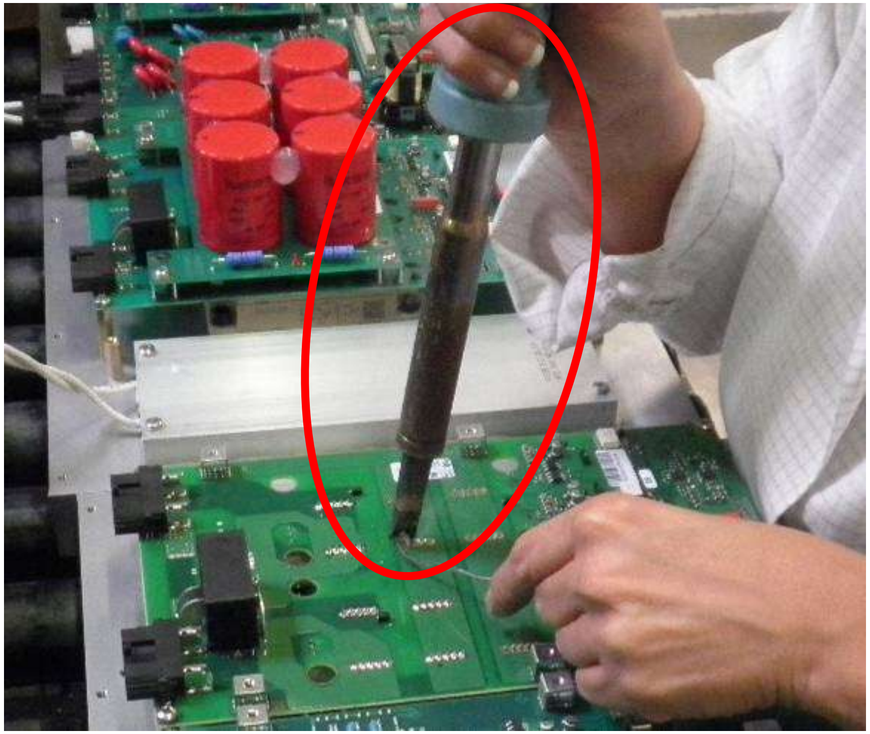
Repair : Soldering in practice





IPC categories Mid / High

Keywords:	Pb-free FR-4	High T_d	T_d (°C)	T_{260} (min)	T_{288} (min)	Low CTE_z	max (%)	T_g (°C)	Moisture Absorp. (%).
/99	Pb-free FR-4	High T_d	≥ 325	≥ 30	≥ 5	Low CTE_z	≤ 3.5	≥ 150	≤ 0.5
/101	Pb-free FR-4		≥ 310	≥ 30	≥ 5	Low CTE_z	≤ 4.0	≥ 110	≤ 0.5
/121	Pb-free FR-4		≥ 310	≥ 30	≥ 5	Low CTE_z	≤ 4.0	≥ 110	≤ 0.5
/122	Pb-free FR-4		≥ 310	≥ 30	≥ 5	Low CTE_z	≤ 4.0	≥ 110	≤ 0.8
/124	Pb-free FR-4	High T_d	≥ 325	≥ 30	≥ 5	Low CTE_z	≤ 3.5	≥ 150	≤ 0.5
/125	Pb-free FR-4	High T_d	≥ 325	≥ 30	≥ 5	Low CTE_z	≤ 3.5	≥ 150	≤ 0.8
/126	Pb-free FR-4	High T_d	≥ 340	≥ 30	≥ 15	Low CTE_z	≤ 3.0	≥ 170	≤ 0.5
/127	Pb-free FR-4		≥ 310	≥ 30	≥ 5	Low CTE_z	≤ 4.0	≥ 110	≤ 0.8
/128	Pb-free FR-4	High T_d	≥ 325	≥ 30	≥ 5	Low CTE_z	≤ 3.5	≥ 150	≤ 0.8
/129	Pb-free FR-4	High T_d	≥ 340	≥ 30	≥ 15	Low CTE_z	≤ 3.5	≥ 170	≤ 0.5
/130	Pb-free FR-4	High T_d	≥ 340	≥ 30	≥ 15	Low CTE_z	≤ 3.0	≥ 170	≤ 0.8
/131	Pb-free FR-4	High T_d	≥ 340	≥ 30	≥ 15	Low CTE_z	≤ 3.5	≥ 170	≤ 0.8

Example : powerboard

PCB	power1	mm
Thickness	D	1,6
Drilled hole diameter	d	0,37
plating thickness	t	0,02
Via Stress Factor	VSF	**8,94**

Process	Counts for
HASL finish	2
Reflow	1
Wave solder	1
Touch up repair	1
Sn	**5**
Result:	**BASIC-MID**

repair action	
Component replacement	3
Sn	**8**
Result:	**High**

Field return	
Component replacement	3
Sn	**11**
Result:	**??**

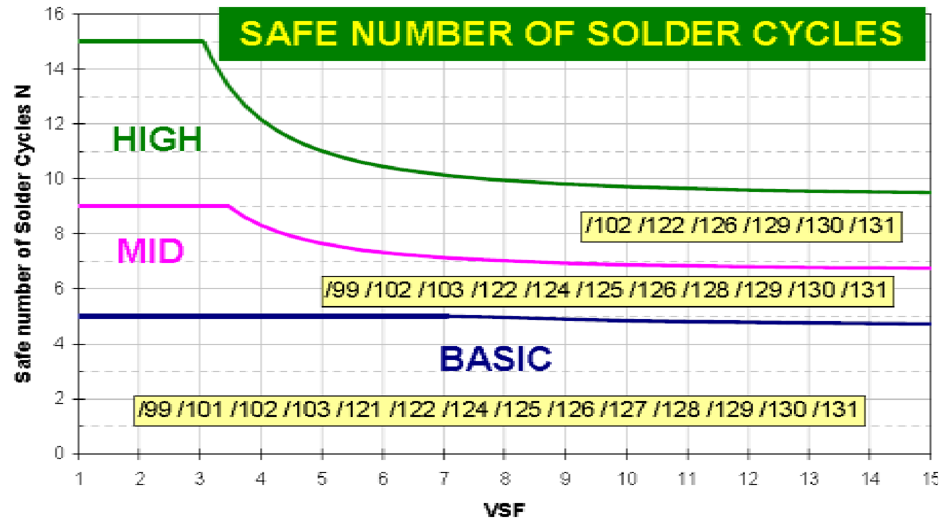


Figure I.16: Safe number of solder cycles for the three thermal performance classes

Keywords:	Pb-free FR-4	High T_d	T_d (°C)	T_{260} (min)	T_{288} (min)	Low CTE_z	max (%)	T_g (°C)	Moisture Absorp. (%).
/99	Pb-free FR-4	High T_d	≥ 325	≥ 30	≥ 5	Low CTE_z	≤ 3.5	≥ 150	≤ 0.5
/124	Pb-free FR-4	High T_d	≥ 325	≥ 30	≥ 5	Low CTE_z	≤ 3.5	≥ 150	≤ 0.5
/127	Pb-free FR-4		≥ 310	≥ 30	≥ 5	Low CTE_z	≤ 4.0	≥ 110	≤ 0.8
/128	Pb-free FR-4	High T_d	≥ 325	≥ 30	≥ 5	Low CTE_z	≤ 3.5	≥ 150	≤ 0.8
/129	Pb-free FR-4	High T_d	≥ 340	≥ 30	≥ 15	Low CTE_z	≤ 3.5	≥ 170	≤ 0.5
/130	Pb-free FR-4	High T_d	≥ 340	≥ 30	≥ 15	Low CTE_z	≤ 3.0	≥ 170	≤ 0.8
/131	Pb-free FR-4	High T_d	≥ 340	≥ 30	≥ 15	Low CTE_z	≤ 3.5	≥ 170	≤ 0.8

Conclusion

- Rework & repair (RMA) must be taken into account for choice of laminate.
- One has to know the scope (limits) of the test(s).
- Tests with good diagnostics –avoid trial & error- help to reduce soldercycles.
- History of the board is important.
- Good workmanship and/or automated (controlled) soldercycles