ON Semiconductor®

Active Components in today's PBA: Challenges for ON Semi

Sept 2011

ON Semiconductor Major Internal Packaging Platforms

CBSM PLATFORM
SMC
SMB
SMA
POWERMITE®
SOD123 Flat Lead

POWER PLATFORM
Power DCA
CASE 77 TO-264 3/5 LD TO-247
TO-218 TO-220 3/5 LD
TO-3P

SOSM PLATFORM
•Thermally Enhanced
•Ultra Thin SOSM Pkg
DPAK 3/5 LD
D2PAK 3/5/7 LD
Power MCP
SO8/DPAK LL/FL Clip Bond
ChipFET™
US8
SOD723
SC82
SC75
TSOP5
Micro8™
SC74
SOD123
SOT23
SOD923
SOT9x3
SOT723
SOT-1123

LPSM PLATFORM
SC89
SOT5x3
SOD323
SC88/A
SC70
TSOP6
SOT223
SOD523

QFN PLATFORM
•Ultra Thin QFN
LQFP EP 52/64
LQFP/TQFP
SOIC W EP 16/24
TSSOP 14/16/20/24/28
SOIC W 16/20/24/28
SO8 TMOS
SOIC N 8/14/16
8080-52
6050
4040-24
3333 Dual
3030-16L
3030-10L
3030-06L
2022
2020
1616
1210
1010

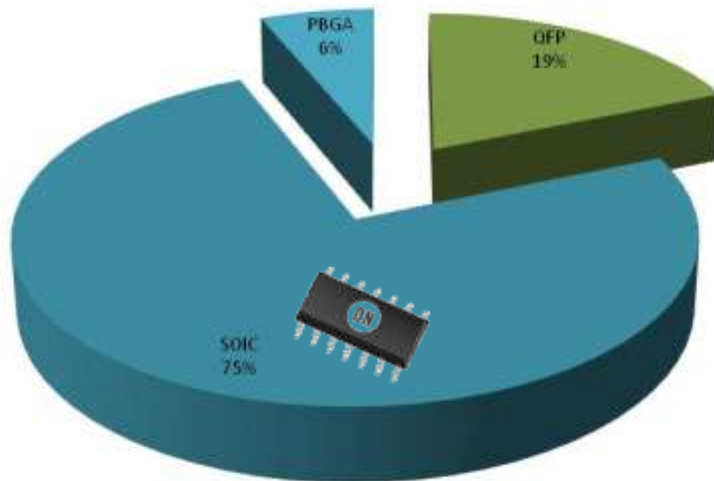
WLP PLATFORM
9002
4107
4685/6 4717
2890/ 4894/6
3101
4103

Major Internal Packaging Platforms

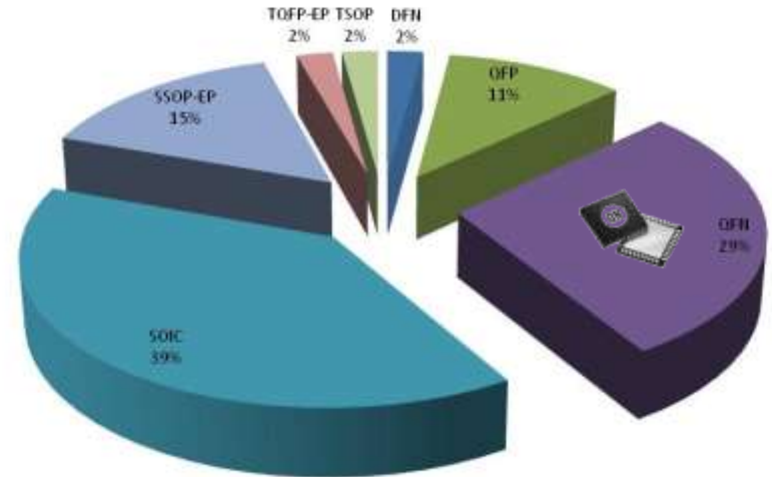
- Primary Push towards Exposed Pad Packages in SOSM and LPSM Platforms
- Increased Emphasis on Multiple and Stacked Die in LPSM and QFN platforms
- Green BOM available for all platforms

Package Trend for Active Automotive Components

2005



2011



Observations:

- 31% leadless packages versus 0% in 2005
- 48% exposed pad packages – thermal management
- 39% quad packages versus 19% in 2005

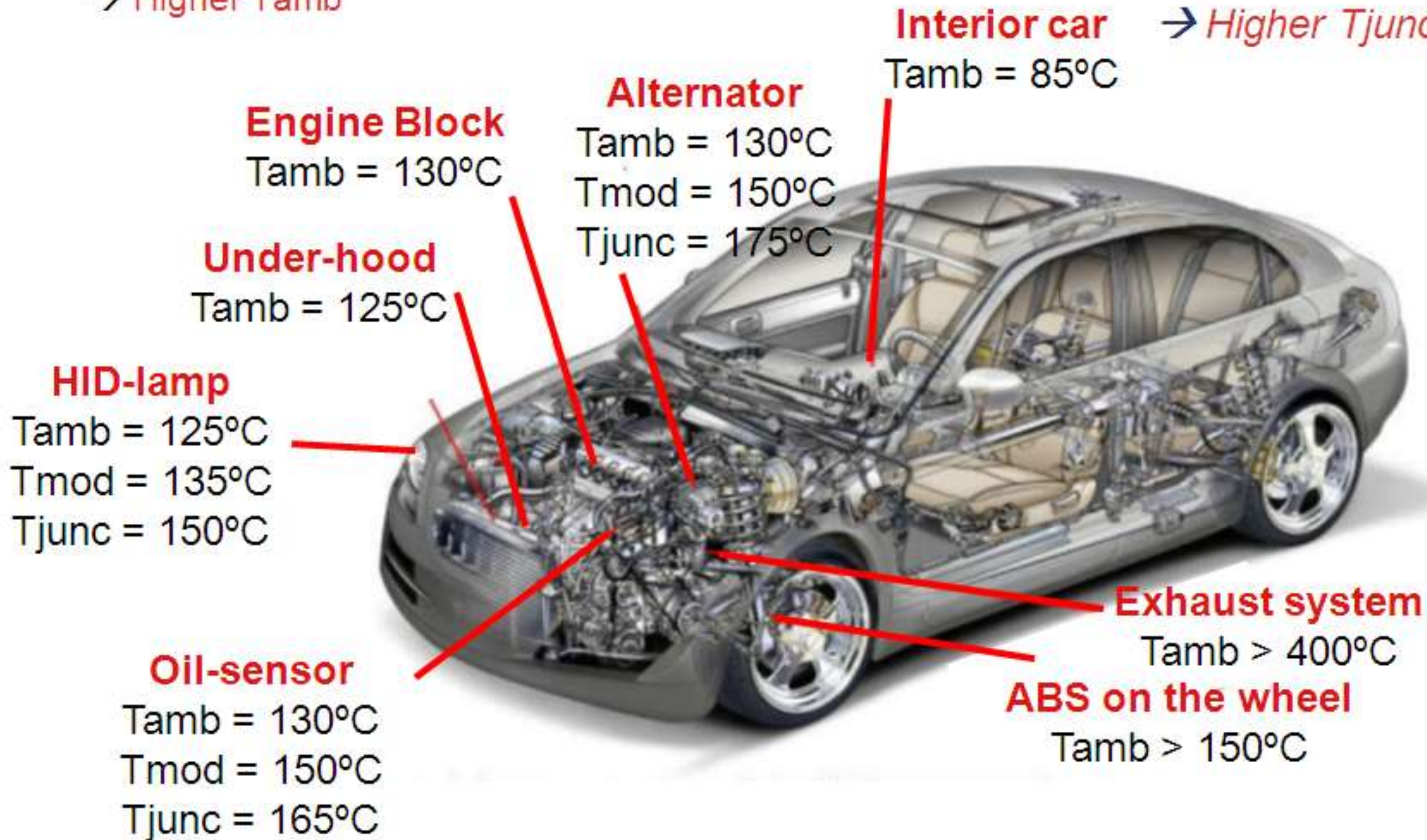
⇨ Significant increase of leadless packages
⇨ Significant increase of exposed pad packages

Package Trend Drivers

Push to higher junction temperature

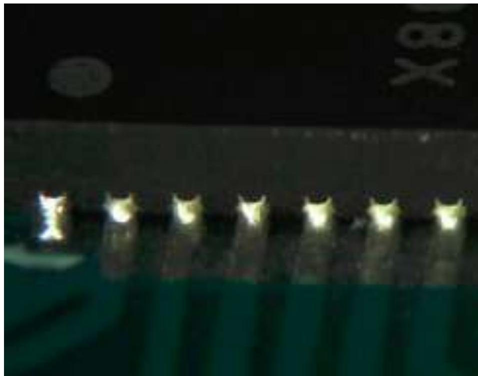
Applications under the hood
→ Higher Tamb

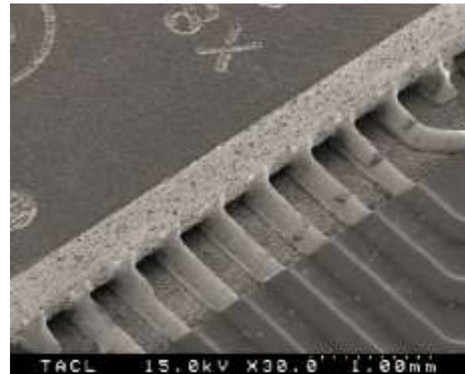
Mechatronic-modules
→ *Higher Tmod*
Higher integration level
→ *Higher Tjunc*

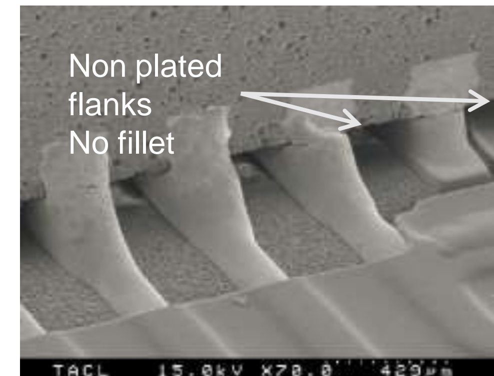


Package Trend Drivers

- Thermal performance improvement
  - ⇨ higher power density/mm2 silicon
  - ⇨ higher current densities
- Reduction in board area & weight
- Height reduction
- Green bill of materials
- AEC-Q100 compliancy
- Leadless packages to have visual solder inspection capability
  - ⇨ QFN/DFN packages with wettable flanks



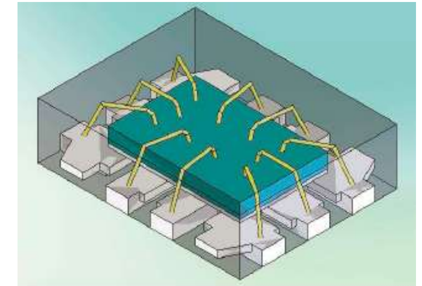


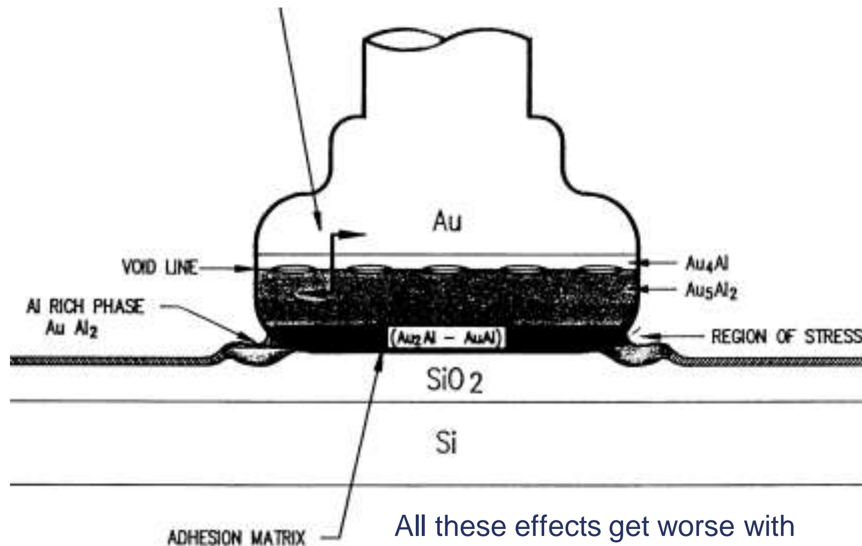


Challenges New Package developments

High temperature design - Main issues:

- Most reliability failures increase **exponential** with temperature
- Wire bond reliability decreases **exponential** with temperature and more then linear with current
- Junction and sub-threshold leakage increase **exponential** with temperature and create new circuit failure types
- Hot spots can create locally accelerated wear out





All these effects get worse with increasing temperature ! (reported acceleration coeff. for 200 degC is 6 X higher than for 150 degC)

1) Formation of brittle intermetallics

Mismatch between TCE of Au5Al2 and Au4Al

2) Kirkendal voiding due to un-equal inter-diffusion of 2 bond metals

Au diffuses more rapidly in Al than reverse

3) Voiding due to electro migration in bondpad metal

Only for negative currents through bond

4) Dry corrosion of intermetallics

With flame retardants (Br) in mold compound as catalyst

Other risks: melting

⇨ **Leading to increase in electrical resistance / loss of bond strength**

Challenges New Package developments

High temperature design - Challenges:

- ⇨ control high temperature aging of wire bond interconnect
- ⇨ estimate expected life time

How ?

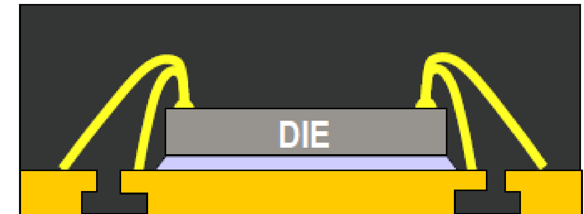
- ⇨ wire bond reliability life time calculator
- ⇨ Tool to calculate wire bond life time based on junction temperature and duration
- ⇨ Computations based on
  - ⇨ physical reliability test results
  - ⇨ test to fail in order to create Weibull distribution
  - ⇨ FMA to understand root cause of failures
  - ⇨ extract activation energy and apply Arrhenius law to calculate life time expectation

Tjunction	Cumulative life time.
175	500h
150	5000h
125	10000h
100	
75	40000h
50	
25	
0	
-40	40000h

Challenges New Package developments

Good temperature cycling performance: Challenges

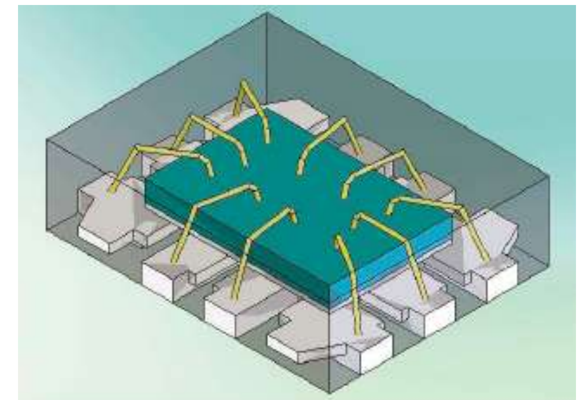
- ⇨ Electrical Cpk >1.76 over entire temperature range
- ⇨ No electrical failure after TC -65/+175 degC for 500 cycles min. (JEDEC standard JESD-104)
- ⇨ Good wire pull (3gr min.) and ball shear test results after TC test with Cpk >1.33



How ?

- ⇨ BOM selection with minimal CTE mismatch
- ⇨ Limit stress variations over the silicon
- ⇨ Tight process control in assembly

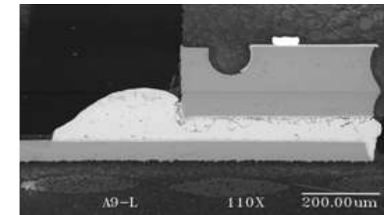
Component	Material	Thermal Conductivity (W / m * K)	CTE (ppm / C)	Glass Transition Temp. (C)
Semiconductor	Silicon	120	2,3	-
leadframe	C194	259	17,6	-
Die Attach Adhesive	Non Conductive Epoxy	0,4	44/136	36
	Conductive epoxy	1,6	81/181	38
Bondwire	Gold 1.0 mils	260	14,2	-
Encapsulation	Mold Compound	1	8/39	130

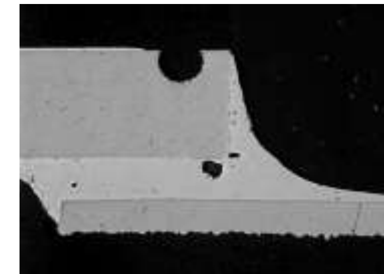


Challenges for ON Semi
Board Level Reliability Performance of Leadless Packages

QFN/DFN Package characteristics:

- No external package leads
- Limited solder contact area
- No solder meniscus or fillet with standard QFN/DFN
- QFN/DFN with wettable flanks is optional





Solder Joint Reliability depends on:

- Proper PCB material / parameter selection
  - Board thickness
  - Board finish
  - Thermo mechanical properties of the PCB
- Proper PCB footprint design
- Proper Surface mount assembly
  - solder material selection
  - solder height
  - solder process

Not ONSEMI's core business

- Package design and bill of materials
- Die size versus package size

ONSEMI's core business

Challenges for ON Semi

Better understand customer PBA reliability expectations

- Board level reliability expectations to be reviewed with customers at project start
- Selected packages to be aligned with PBA reliability expectations
- Understand:
  - today's PBA issues
  - the interaction of PBA and components
  - available scientific information related to PBA issues
  - build network with field experts

⇨ ON SEMI became EDM Partner