



# ASML

## Predictable Initial Product Performance

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Bits en Chips 2011

# Agenda

- Introducing ASML – a cornerstone of the chip industry
- Chip industry drivers
- Strategy Consequences
- Initial Product performance



A decorative graphic consisting of numerous thin, light blue curved lines that sweep from the bottom left towards the top right, creating a sense of motion and depth. The lines are more densely packed on the right side, where they converge into a solid blue shape.

# Introducing ASML, a cornerstone of the chip industry

Public



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# Our strategy



To be a technology leader in lithographic systems and software for semiconductor manufacturing, thus enabling our customers to increase the functionality of microchips while reducing the cost and power consumption per function on a chip



# ASML Headquarters in Veldhoven



July 11, 2011

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# The chip industry drivers

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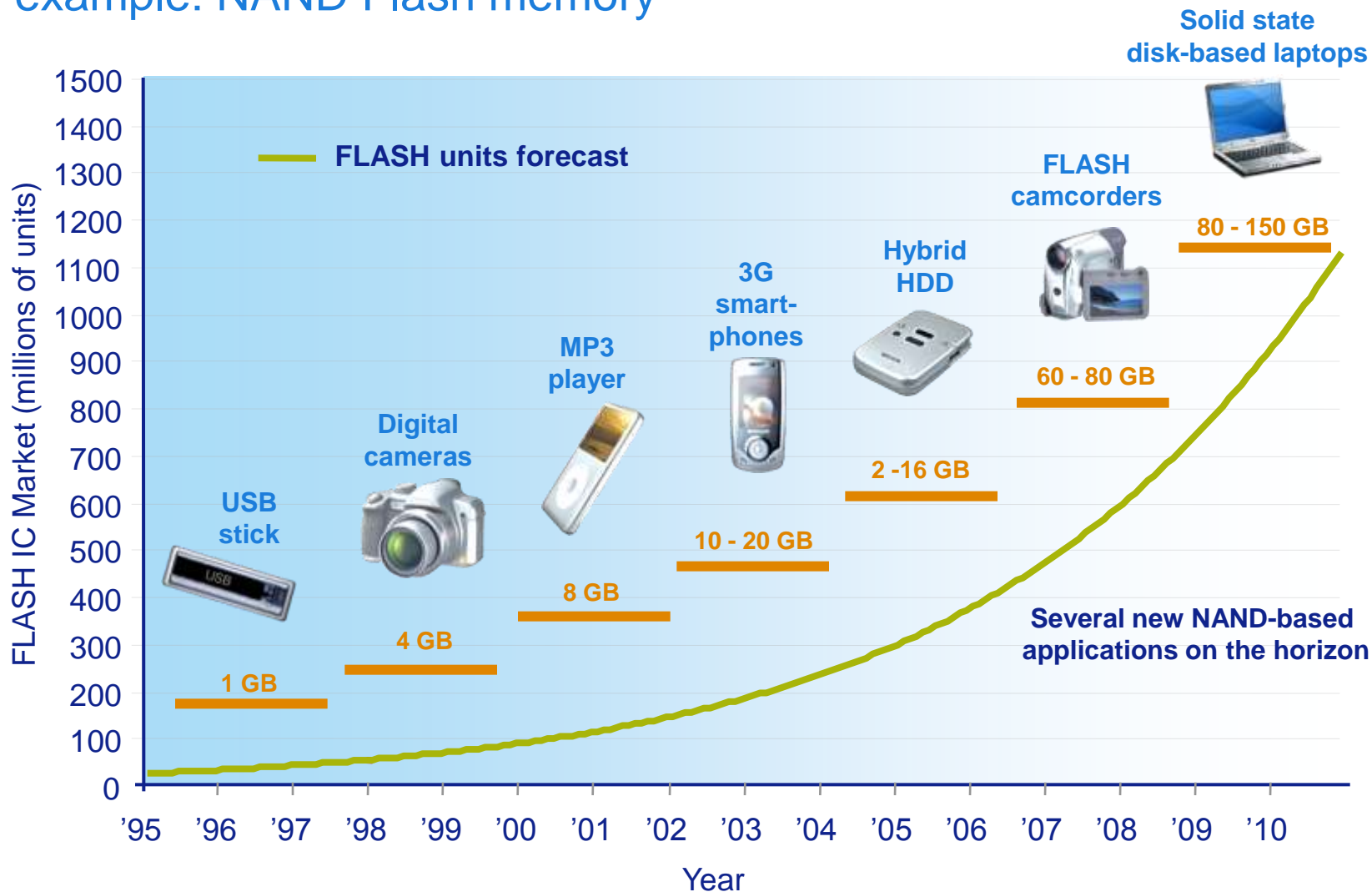
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# Smaller and cheaper chips mean market growth

example: NAND Flash memory



Source: ASML MCC, WSTS, Gartner

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# Strategy Consequences

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# Systems that conquered the market

In 30 years: From 1,200 nm to less than 20 nm resolution

From <0.5M€ per system to >60M€



**1984:**  
**PAS 2000**

Resolution:  
>1µm

overlay:  
250 nm



**1989:**  
**PAS 5000**

Resolution:  
<500 nm

overlay:  
100 nm



**1990's:**  
**PAS 5500**

**steppers/scanners**

Resolution: 400 to 90 nm

overlay: 100 to 12 nm



**2000's:**  
**Twinscan**

Resolution:  
100 to 38 nm

overlay: 20 to 4 nm



**2010's:**  
**NXE EUV systems**

Resolution:  
32 to <20 nm  
overlay: 2 nm



# Complexity increase needed to accommodate performance



**1984:**  
**PAS 2000**

120 PCBA's  
DIL's



**1989:**  
**PAS 5000**

250 PCBA's  
DIL's



**1990's:**  
**PAS 5500**  
**steppers/scanners**

600 PCBA's  
SMD



**2000's:**  
**Twinscan**

800 PCBA's  
Ball grids



**2010's:**  
**NXE EUV systems**

1200 PCBA's  
uBall grids



# Time and space required to build a system



**1984:**  
**PAS 2000**

Proto build



**1989:**  
**PAS 5000**  
12 weeks/12sqm



**1990's:**  
**PAS 5500**  
steppers/scanners  
12 weeks/40sqm



**2000's:**  
**Twinscan**  
16 weeks/70sqm



**2010's:**  
**NXE EUV systems**  
35 weeks/ 250sqm



# Strategy Consequences

- Limited number of machines
- Complexity increase per platform
- Increased Number of parts
- Machine Build time
- Machine Space requirements



# Strategy Consequences

- Limited Number of machines (50/year)

- Total PCBA Serie size 100 – 300
  - Learning period is too long

- Complexity Increase

- 1200 PCBA's per machine (2010)
- 100 – 4000 parts/PCBA
  - Current Zero hour defect rate (high mix - low volume) <1%



# Strategy Consequences

## •Machine Build Time

- Machine build time disturbances (12 disturbances/machine)
  - Clean room space occupation
  - Interest loss over 35M €
- Spare parts
  - Customer machine down time





# Initial Product Performance

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# Required Initial Product Performance

- 1 Disturbance per machine build (Electronics)
  - 1200 PCBA's per machine & Limited series
    - PCBA Zero hour defect rate (high mix - low volume) <0.1%





# Product performance

- Predictable performance of PCBA's
  - With 1 Disturbance during machine build
    - Cycle time reduction
    - Lower Total cost of PCBA (Test + product cost --)
    - Less clean room space
    - Less interest loss
    - Less handling defect products (DOA's)
  - Better discussion Test Cost versus Zero hour defects (0.1%)
    - From opportunistic testing -> Structured risk mitigation



# Questions

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