Modeling the Low- and High-Frequency Impedance of Thermal Reliefs

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***Abstract*—Thermal reliefs are structures that decouple a via thermally from a large conductor plane and as such create a thermal barier in order to obstruct heat conduction through these planes during the soldering process.**

Two models have been developed that describe the impedance of a thermal relief structure at DC and at RF. The first model gives an estimate of the excess resistance that is added by introducing a thermal relief on the connection of a hole to a large conductor plane, which is directly related to the thermal resistance. The second model estimates the excess inductance that is introduced in the connection by the thermal relief at RF frequencies.

I. Introduction

The generic standard on Printed Circuit Board Design (IPC 2221 [1]) states that thermal reliefs are required for holes that are subject to soldering in large conductor areas such as ground planes, power planes and thermal planes. Thermal reliefs create a thermal barier which avoids heat to conduct away from the soldering joint through these planes and causing a cold soldering joint.

In general thermal reliefs are recommended for printed board assembly (PBA). However, signal and power integrity (SI and PI) engineers often keep thermal reliefs out of their designs because they are concerned with possibly unacceptable voltage drops between the component pin and the conductor plane, as well at DC as at RF operation. Although limited information is available, Printed Circuit Board (PCB) designers do not dispose of general tools that can be used to assess the thermal and/or electrical properties of the thermal relief during soldering and normal operation. Moreover, almost no references are available that are concerned with the SI, PI and EMC behaviour of thermal reliefs at low (DC) and RF frequencies.

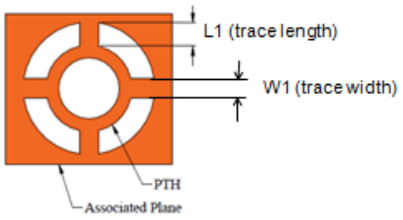


Fig. 1. Lay-out of a (circular shaped) thermal relief

A thermal relief structure is shown in Figure 1 and consists of a circular pad that connects to a large plane through four small traces or spokes, also referred to as the web in IPC-2221/IPC-2222 [1], [2]. The shape of a thermal relief can be circular or rectangular. Adding a thermal relief means adding a thermal resistance between the via barrel and the plane which the thermal relief connects to. Most commonly thermal reliefs are applied for through-hole (TH) components. In case no thermal reliefs are present on the connections to large conductor planes, during the wave-soldering process, the heat will conduct through these large planes away from the soldering joint. This can cause an inreliable weak soldering joint. In some cases, thermal reliefs are also added where Surface Mount Technology (SMT) components connect to large conductor planes and reflow soldering is used. These structures are mostly referred to as thermal pads or thermal ties. In case of very small SMT components, tombstoning can occur. Tombstoning is the process where one end of the SMT component raises from the solder paste due to an imbalance in the wetting forces during reflow soldering.

PBA guidelines recommend adding thermal reliefs at the connections between TH-pins and large conductor planes to ensure reliable solder joints. Nevertheless, PI-, SI- and EMC-(Electromagnetic Compatibility) engineers are often concerned with the voltage drop that is introduced by these structures. As stated earlier, only a few references are available in literature. IPC-2222 [2] gives a more detailed discussion on the dimension of thermal reliefs, but does not give a physical explanation or quantification of their outcomes. A US patent [3] exists that describes thermal reliefs that are optimized for Electromagnetic Interference (EMI), claiming that the shape of these thermal reliefs reduces RF phenomena such as reflections at the aperture boundaries. However, no quantification is given. Other references [5], [6] discuss only the thermal characteristics and the contradiction between (thermal) demands during soldering and normal operation of the printed board design. In [5], a (thermal) design guideline is given that optimizes the design both for soldering and normal operation, based on the

transient behaviour of thermal reliefs. It is concluded to use four wide spokes and a large pad-to-plane clearance.

This lack of quantification has lead to different myths and a wide spread of diverse guidelines amongst PCB designers considering the use of thermal reliefs. This paper discusses and quantifies the impedance of thermal reliefs and formulates two empirical expressions that can be used by PCB designers to estimate the DC resistance and inductance of a circular thermal relief (see Figure 1), which is most common. In this paper, only TH-technology is considered. Due to the inductance of the via itself that becomes dominant at higher frequencies, the frequency range from 0 to 800MHz is analyzed, allowing a quasi-static analysis of thermal relief structures. The build up of a thermal relief is discussed in section II.

II. Model of a thermal relief

The thermal relief, discussed in this paper (see Figure 1), consists of one or several thin spokes that connect the via land to a large conductor plane through small traces, also called the web of the thermal relief. The shape of the web will determine the impedance of the thermal relief. Two different models have been developed: one for the DC resistance and one for the RF impedance of the web. At DC, the conductor properties and thickness are important parameters which need to be incorporated in the model. At RF frequencies, it can be assumed that the current only flows in a small outer region of the conductor. This allows to neglect the internal inductance of the thermal relief and thus to represent the conductors as thin perfect conductors (PEC). This assumption allows a simplification of the simulation model.

Analytical formulas have been developed based on full-wave simulations. The DC model has been validated using a stationary current solver [7], while for the RF model, a quasi-static method-of-moments technique [8] has been used to extract, parameterize and curve-fit the equivalent impedance of the thermal relief.

III. The impedance of thermal reliefs

A. DC Resistance

The electrical resistance of a conducting structure is closely related to its thermal resistance. Due to thermal requirements of the manufacturing process of the PCB, it is a main design parameter for the PCB designer. If electrical and thermal models are available, the lay-out can be optimized to reduce the voltage drop (and equivalently the power dissipation during normal operation) while still satisfying the thermal requirements for manufacturing. An empirical formula is fitted to full-wave simulation data of the DC resistance, which includes six parameters:

- Spoke length (L) [mm]
- Spoke width (W) [mm]
- Conductor thickness (T) [mm]
- Via radius (R) [mm]
- Number of spokes in the web (N) []
- Conductivity of the conductor (C) [S/mm]

TABLE I
DC coefficients

b_1	b_2	b_3	b_4	b_5	b_6
1.7005	0.2043	0.1489	1.3021	0.9886	1.0018

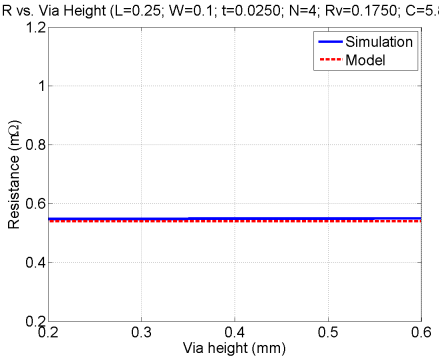


Fig. 2. DC Resistance of a thermal relief vs. Via Height

The expression that has been fitted follows below:

$$R_{DC}\,[\Omega] = [b_1 \cdot L + b_2] \cdot \left[\frac{R^{b_3}}{N^{b_4}}\right] \cdot \left[\frac{1}{W^{b_5}}\right] \cdot \left[\frac{1}{T^{b_6}}\right] \cdot \left[\frac{1}{C}\right] \quad (1)$$

From the full-wave simulations, it is noted that the dependence of the DC resistance of the thermal relief on the via height is negligible. This is shown in Figure 2. In curve-fitting it has been assumed that the function is separable in its parameters. In L and ρ ($\rho = \frac{1}{C}$), a linear behaviour is assumed. Based on the results of curve-fitting, power functions are suitable to represent the trend of the resistance in function of R, N, W and T. The fitted coefficients are tabulated in table I. From the table, one notes that the coefficients that come with W and T are almost 1. This means that the DC resistance is purely inverse with regard to W and T, which slightly simplifies the expression above. The formula can then be read as:

$$R_{DC} = C_1 \cdot \frac{\rho \cdot [C_2 \cdot L + 1]}{A} \quad (2)$$

Equation (2) links to the resistance of a conductor of uniform cross-section [9] with length L and cross-section $A = W \cdot T$ with 2 correction factors that compensate for the influence of the circumference of the via and the shape of the web (number of spokes). It is noted that the resistance is not exactly inversely proportional to the number of spokes.

The model is fitted on data achieved in the region of validity as given by table II. This region is chosen based on input from PCB designers and from the assumption that only TH-technology is considered. The correspondence of the model with the full-wave simulation data is shown in Figure 3 for different sets of parameters.

B. RF Inductance

In the previous section, the resistance of a thermal relief at DC is discussed and an analytical empirical formula has

TABLE II
REGION OF VALIDITY: DC

$L(mm)$	$W(mm)$	N	$T(\mu m)$	$R_v(mm)$	$C(S/m)$
0.1 - 0.5	0.1 - 0.4	2 - 5	25 - 45	0.175 - 0.5	3.5 - 6.375 $\times 10^7$

TABLE III
RF: PARAMETER SELECTION

$L(mm)$	$W(mm)$	N	$R_v(mm)$	$H(mm)$	$L_{eq}(pH)$
0.25	0.1	1	0.175	0.2	220
0.25	0.1	2	0.175	0.2	93
0.25	0.1	3	0.175	0.2	52
0.25	0.1	4	0.175	0.2	31
0.25	0.2	4	0.175	0.2	21
0.25	0.3	4	0.175	0.2	13
0.25	0.1	4	0.250	0.2	36
0.25	0.1	4	0.325	0.2	39
0.50	0.1	4	0.175	0.2	51
0.25	0.1	4	0.175	0.6	38
0.25	0.1	4	0.175	1.0	37

been formulated which can be used to analyse the influence of a thermal relief on the voltage drop that will occur at the soldering joint. In the case that RF currents flow down the through-hole joint through a thermal relief to the conductor planes, an additional voltage fluctuation will occur due to the

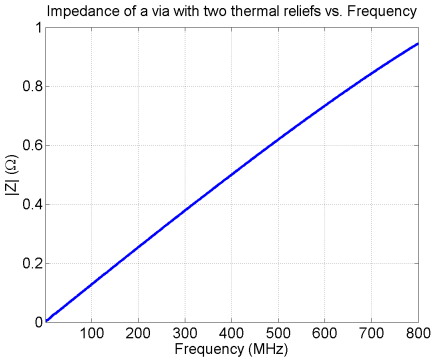


Fig. 4. Impedance of a via connected to two large conductor planes through two thermal reliefs

RF impedance of a thermal relief. In Figure 4, the magnitude of the complex impedance of a small via that connects to two large conductor planes through respectively two identical thermal reliefs is shown. It is seen that up to 800MHz, the impedance is approximately linearly proportional to the frequency, which suggests that a thermal relief behaves mainly as an inductive component. Therefore, this section describes the equivalent inductance of a thermal relief, and neglects the small equivalent capacitance of the thermal relief.

The same parameters can be used as in the DC model. however, in order to simplify the model, it is investigated

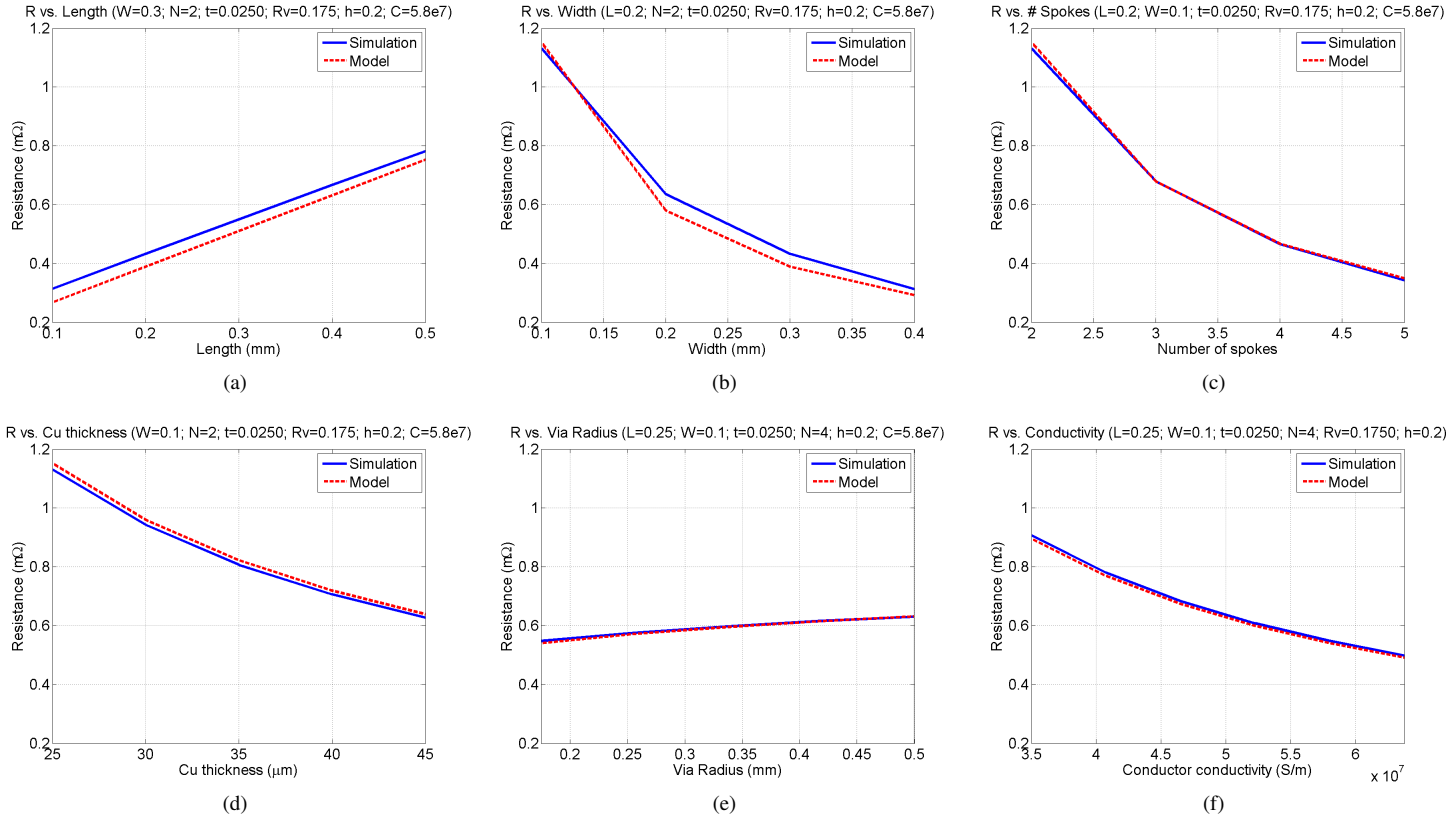


Fig. 3. Thermal relief - DC Resistance vs. Leg length(a); Leg Width(b); Number of Spokes(c); Conductor thickness(d); Via Radius(e); and Conductivity(f).

which parameters are the main contributors to the inductance variation of a thermal relief. An equivalent inductance value is fitted to a set of simulation samples as shown in table III. It is seen that the length, width and number of spokes play a major role in the inductance of the thermal relief, while the height and the radius of the via play a minor role. Fluctuations of $3pH$ correspond to an equivalent impedance variation of only $2.5m\Omega$ at $800MHz$. According to rules of thumb [9], the loop inductance of $0.2mm$ spaced conductor planes approximates $250pH/square$ and the inductance of a $0.25mm$ diameter wire approximates $1nH/mm$. This means that in the regular TH-technology range, these small fluctuations can be neglected, but when a detailed model at higher frequencies is needed, these fluctuations have to be taken into account. However, the accuracy of the full-wave simulation will be discussed further on. An analytical empirical formula is fitted to the full-wave data which only contains three parameters:

- Spoke length (L) [mm]
- Spoke width (W) [mm]
- Number of spokes in the web (N) []

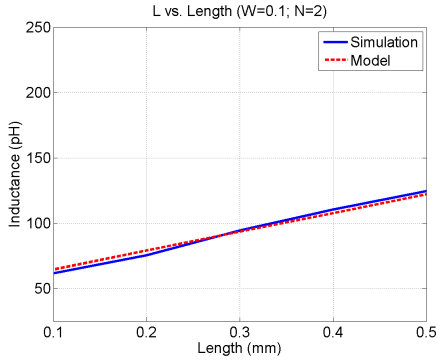
Based on curve-fitting of the trends of the inductance in function of these three parameters, the following non-linear function is proposed:

$$L_{eq}\,[pH] = b_1 \cdot (L + b_2) \cdot \left[\frac{W^{-b_3}}{W + b_4}\right] \cdot \left[\frac{N^{-b_5}}{N + b_6}\right] \qquad (3)$$

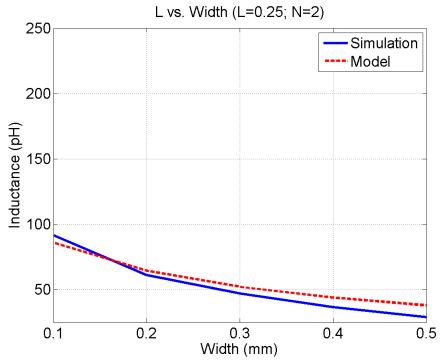
The link with a physical derivation is less clear than in the DC case. It is seen that the inductance has a complicated behaviour in function of the width and the number of spokes. The fitted coefficients are found in table IV. As in the DC case, inductance is not perfectly inversely proportional to the number of spokes.

The model is compared with the simulation results in Figure 5. A good correspondence is seen for the behaviour in function of L and N, however the behaviour in function of W shows a small discrepancy between model and simulation for large values of W. This can be accounted for by the very low value of the inductance in this case (around 30pH), which puts high demands on the accuracy of the full-wave simulation model (the accuracy of the used mesh discretization). It was seen that the result was very sensitive to small differences in the mesh between the models with and without thermal reliefs. Special measures were applied in order to minimize this error. Another source of error is introduced in the model by de-embedding the impedance of the large conductor planes in order to extract the equivalent impedance of the via. In table V, the region of validity of the RF model is given. The boundaries are slightly different than for the DC case. This is due to modeling limits in the full-wave simulations.

A more practical case has been modeled to investigate the influence of the presence of thermal reliefs on the RF performance of a design. The case of 4 decoupling capacitors is discussed that connect to a large power and a large reference plane. On both planes, thermal reliefs are added to the soldering joints of all capacitors. The geometry is shown in Figure 6. Because TH-technology is considered, the maximum frequency of interest is set to 800MHz. The length and width of the thermal relief spokes equal respectively $0.25mm$ and $0.1mm$, the via radius equals $0.175mm$. The extracted equivalent inductance is tabulated in table III. The thermal reliefs are assumed to be perfectly conducting (PEC). The results are shown in Figure 7. It is clearly seen that the thermal reliefs have a negligble effect on the RF impedance of the decoupling capacitors in the frequency range of interest if the web of the thermal relief consists of at least two spokes. In case only one spoke is used, the impedance is increased above the first resonance frequency.



(a)



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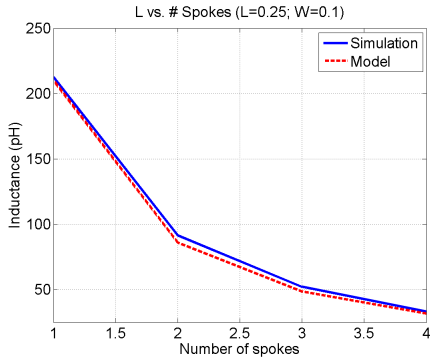

(c)

Fig. 5. Thermal relief - Inductance vs. Leg length(a); Leg Width(b); and Number of Spokes(c).

TABLE IV
RF COEFFICIENTS

b_1	b_2	b_3	b_4	b_5	b_6
497.81	0.34626	0.21754	0.58135	0.91737	2.422

TABLE V
REGION OF VALIDITY: RF

$L(mm)$	$W(mm)$	N
0.1 - 0.5	0.1 - 0.5	1 - 4

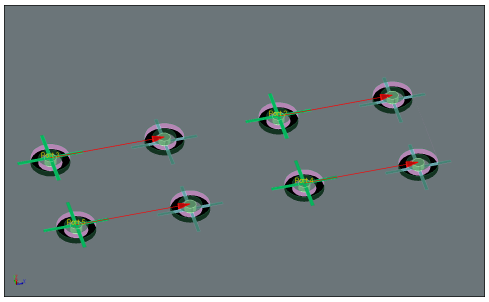

Fig. 6. Geometry of test case: 4 decoupling capacitors with and without thermal reliefs

IV. CONCLUSION

In this paper, the impedance of thermal relief structures is discussed. Due to very limited access to a quantification of the SI, EMC and thermal characteristics of thermal reliefs, different myths exist whether to add or leave out thermal reliefs in printed board design. Above, two empirical formulas have been fitted to full-wave simulation data of the impedance of thermal reliefs. Both the DC resistance as the RF impedance are important factors which are of practical interest to the PCB designer.

The obtained expression for the DC resistance is seen to be linked to the analytical formula for the resistance of a uniform conductor and gives a good correspondence to the full-wave simulation results. The expression describing the RF inductance depends on a smaller set of parameters then the expression for the DC resistance, however it still provides satisfying results. The expression for the RF inductance looks more complicated and is not directly correlated with a simplified physical equivalent.

The DC resistance of regular thermal reliefs ranges from a tenth to one miliohm, and the RF inductance ranges from a few tenths to a few hundredths picohenries. Depending on the demands of the application, the added DC resistance and inductance can be kept low by appropriately designing the thermal relief. This is also shown in an example of 4 decoupling capacitors wich are connected to large conductor planes on a PCB using thermal reliefs.

It is confirmed that thermal reliefs do not imply a problematic issue in general PCB designs for SI, PI or EMC. This can explain the limited information that is available in scientific literature. However, in high-current applications or in sensitive

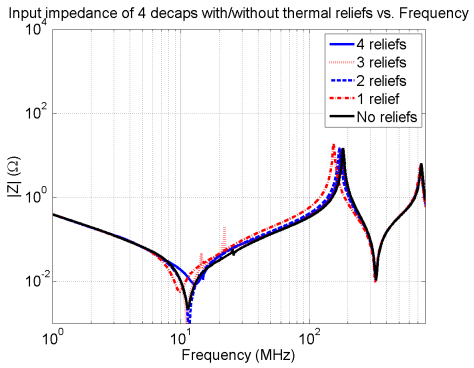

Fig. 7. Input impedance of 4 decoupling capacitors with and without thermal reliefs

RF designs, it can be useful to have access to a model that estimates the impedance of thermal reliefs, and which can be used as a design parameter to optimize the printed board design.

Future work should handle the correlation of the empirical expressions with the physics behind thermal reliefs. In this manner, the formulas can be optimized, the dependencies on the different parameters can be investigated more thoroughly, allowing to formulate more general expressions and perform a more general validation. Secondly, thermal pads will be considered that are used to connect SMT compoments to large conductor planes. As they are applied at higher frequencies, a more accurate RF model will be necessary, including also the effects of the pad size.

ACKNOWLEDGMENT

This research was partially funded by the IWT (Flanders, Belgium) under the VIS-Prosperita project.

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